1. A multiple interconnected integrated circuit chip structure comprising a first integrated circuit chip and a second integrated circuit chip comprising:

whereby the first integrated circuit chip is mounted to the second chip to physically and electrically connect the first integrated circuit chip to the second integrated circuit chip;

whereby the first integrated circuit chip has interchip interface circuits connected to the second integrated circuit chip to selectively communicate between internal circuits of the first and second integrated circuit chips and test circuits connected to internal circuits of the first integrated circuit chip to provide stimulus and response to said internal circuits;

whereby the second integrated circuit chip has input/output interface circuitry to communicate with external circuitry connected to said second integrated circuit chip and to protect said second integrated circuit chip from electrostatic discharge voltages;

whereby the interchip interface circuitry comprises:

an internal interface circuit for transferring electrical signals between the second integrated circuit chip and the first integrated circuit chip;

a mode select switch having a first terminal connected to an input/output pad, a second terminal connected to the

internal circuitry of the integrated circuit chip, a third terminal connected to test circuits, and

a mode selector to selectively connect the output of the internal interface circuit to the internal circuitry of the first integrated circuit chip during normal operation and the output of the internal interface circuit to the test circuitry during test and burn-in.

2. The chip structure of claim 1 wherein the second integrated circuit chip further has interchip interface circuits connected to the first integrated circuit chip to selectively communicate between internal circuits of the first and second integrated circuit chips and test circuits connected to internal circuits of the second integrated circuit chip to provide stimulus and response to said internal circuits.

3. The chip structure of claim 1 wherein the first chip is mounted to the second chip by means of an area array of solder bumps.

4. The chip structure of claim 1 wherein the test circuits comprise:

test interface circuits connected to external test circuitry to communicate with said external test circuitry and

ESD protection circuits to protect said first and second integrated circuit chips from electrostatic discharge voltages.

5. The chip structure of claim 1 wherein the first integrated circuit chip is fabricated using a first type of semiconductor process and the second integrated circuit chip is fabricated with a second type of semiconductor process that is not compatible with the first type of semiconductor process.

6. The chip structure of claim 1 wherein the first integrated circuit chip is an array of memory cells and the second integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells.

7. The chip structure of claim 1 wherein the second integrated circuit chip is an array of memory cells and the first integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells.

8. The chip structure of claim 4 wherein the test interface circuit is connected to the external test circuitry through an input/output pad temporarily connected to said external test circuitry during test and burn-in.

9. The chip structure of claim 1 wherein the interchip interface circuit has no electrostatic-discharge-protection-circuit.

10. ~~The chip structure of claim 1 wherein the internal interface circuit is not~~ capable of communication with the external circuitry.

11. The chip structure of claim 1 wherein the mode switch comprises:

a first pass switch having a drain terminal connected to the internal circuits, a source terminal connected to an input/output pad connected to an attached integrated circuit chip, a first gate terminal connected to the mode selector, and a second gate terminal;

a second pass switch having a drain terminal connected to the internal circuits, a source terminal connected to the input/output pad connected to the attached integrated circuit chip, a first gate terminal, and a second gate terminal connected to the mode selector;

an inverter circuit having an input terminal connected to the mode selector and an output terminal connected to the second gate terminal of the first pass switch and the first gate of the second pass switch.

12. The chip structure of claim 10 wherein the first and second pass switches are comprised of an NMOS transistor and PMOS transistor connected in parallel with a gate of the NMOS transistor being the first gate terminal of

the first and second pass switches and a gate of the PMOS transistor being the second gate terminal of the first and second pass switches.

13. The chip structure of claim 1 wherein in the mode switch comprises:

an interchip input/output pad connected to a first logic state generator during normal operation;

a test input/output pad connected to a second logic state generator during testing procedures.

14. An interchip interface circuit formed in multiples upon a first and second integrated circuit chip for communication between internal circuits of the first and second integrated circuit chip;

whereby said first integrated circuit chip is attached physically and electrically to said second integrated circuit chip; and

whereby said interchip interface circuit comprises:

an internal interface circuit for transferring electrical signals between the second integrated circuit chip to the first integrated circuit chip;

a mode select switch having a first terminal connected to an output of the internal interface circuit, a second terminal connected to the internal circuitry of one of the integrated circuit chip, a third terminal connected to test circuits, and a control terminal; and

a mode selector connected to the control terminal to selectively connect the output of the internal interface circuit to the internal circuitry of the integrated circuit chips during normal operation and the output of the internal interface circuit to the test circuitry during testing procedures.

15. The interface circuit of claim 14 wherein the first chip is attached to the second chip by means of an area array of solder bumps.

16. The interface circuit of claim 14 wherein the test circuits comprise:

test interface circuits connected to external test circuitry to communicate with said external test circuitry; and

an ESD protection circuit to protect said first and second integrated circuit chips from electrostatic discharge voltages.

17. The interface circuit of claim 14 wherein the first integrated circuit chip is fabricated using a first type of semiconductor process and the second integrated circuit chip is fabricated with a second type of semiconductor process that is not compatible with the first type of semiconductor process.

18. The interface circuit of claim 14 wherein the first integrated circuit chip is an array of memory cells and the second integrated circuit chip contains

electronic circuitry formed with a process not compatible with a process of the array of memory cells.

19. The interface circuit of claim 14 wherein the second integrated circuit chip is an array of memory cells and the first integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells.

20. The interface circuit of claim 16 wherein the test interface circuit is connected to the external test circuitry through an input/output pad temporarily connected to said external test circuitry during test and burn-in.

21. The interface circuit of claim 14 wherein the interchip interface circuit has no electrostatic discharge protection circuit.

22. The interface circuit of claim 14 wherein the internal interface circuit is not capable of communication with the external circuitry.

23. The interface circuit of claim 14 wherein the mode switch comprises:

a first pass switch having a drain terminal connected to the internal circuits, a source terminal connected to an input/output pad connected to an attached integrated circuit chip, a first gate

terminal connected to the mode selector, and a second gate terminal;

a second pass switch having a drain terminal connected to the internal circuits, a source terminal connected to the input/output pad connected to the attached integrated circuit chip, a first gate terminal, and a second gate terminal connected to the mode selector;

an inverter circuit having an input terminal connected to the mode selector and an output terminal connected to the second gate terminal of the first pass switch and the first gate of the second pass switch.

24. The interface circuit of claim 23 wherein the first and second pass switches are comprised of an NMOS transistor and PMOS transistor connected in parallel with a gate of the NMOS transistor being the first gate terminal of the first and second pass switches and a gate of the PMOS transistor being the second gate terminal of the first and second pass switches.

25. The interface circuit of claim 23 wherein in the mode switch comprises:

an interchip input/output pad connected to a first logic state generator during normal operation;

a test input/output pad connected to a second logic state generator during testing procedures.

26. A method of forming a multiple integrated circuit chip structure comprising the steps of:

simultaneously but separately forming internal circuits on a first semiconductor wafer containing a plural first integrated circuit chips and a second semiconductor wafer containing a plural second integrated circuit chips;

simultaneously forming test circuits on the first wafer and the second wafer;

simultaneously forming interchip interface circuits on the first wafer and the second wafer, whereby forming said interchip interface circuit comprises the steps of:

forming an internal interface circuit for transferring electrical signals between a second integrated circuit chip to a first integrated circuit chip;

forming a mode select switch having a first terminal connected to an output of the internal interface circuit, a second terminal connected to the internal circuitry of the first integrated circuit chip;

forming a mode selector to selectively connect the output of the internal interface circuit to the internal circuitry of the

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first integrated circuit chip during normal operation and the output of the internal interface circuit to the test circuitry during test and burn-in;

forming input/output interface circuits on said second wafer;

contacting, stimulating, and examining a response of the test circuits on the first wafer and the test circuits and input/output interface circuits on the second wafer;

separating the first wafer into a plurality of separated first integrated circuit chips;

contacting with sockets, stimulating and burning-in the plurality of separated first integrated circuit chips for an extended period of time;

contacting, stimulating, and examining the plurality of separated first integrated circuit chips;

discarding defective first integrated circuit chips;

attaching each functioning chip of the first integrated circuit chips to ~~one of one~~ a functioning second integrated circuit chip on the second wafer;

separating the second wafer into the plurality of second integrated circuit chips; and

contacting the input/output interface circuits, stimulating, and examining the response of the formed multiple integrated circuit chip structure.

27. The method of claim 26 wherein the attaching of each of the first integrated circuit chips to the second integrated circuit chips is accomplished by forming a area array of solder bumps between each of the first integrated circuit chips and the second integrated circuit chips.

28. The method of claim 26 wherein forming the test circuits comprises the steps of:

forming test interface circuits connected to external test circuitry to communicate with said external test circuitry and

forming ESD protection circuitry to protect said first and second integrated circuit chips from electrostatic discharge voltages.

29. The method of claim 26 wherein the first integrated circuit chip is fabricated using a first type of semiconductor process and the second integrated circuit chip is fabricated with a second type of semiconductor process that is not compatible with the first type of semiconductor process.

30. The method of claim 26 wherein the first integrated circuit chip is an array of memory cells and the second integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells.

31. The method of claim 26 wherein the second integrated circuit chip is an array of memory cells and the first integrated circuit chip contains electronic circuitry formed with a process not compatible with a process of the array of memory cells.

32. The method of claim 26 wherein contacting the test interface circuit comprises the step of temporarily connecting external test circuitry through an input/output pad to said test interface circuit.

33. The method of claim 26 wherein the interchip interface circuit is formed with no electrostatic discharge protection circuit.

34. The method of claim 26 wherein the internal interface circuit is formed with no ability to communicate with the external circuitry.

35. The method of claim 26 wherein the mode select switch comprises:

a first pass switch having a drain terminal connected to the internal circuits, a source terminal connected to an input/output pad connected to an attached integrated circuit chip, a first gate terminal connected to the mode selector, and a second gate terminal;

a second pass switch having a drain terminal connected to the internal circuits, a source terminal connected to the input/output

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pad connected to the attached integrated circuit chip, a first gate terminal, and a second gate terminal connected to the mode selector;

an inverter circuit having an input terminal connected to the mode selector and an output terminal connected to the second gate terminal of the first pass switch and the first gate of the second pass switch.

36. The method of claim 32 wherein the first and second pass switches are comprised of an NMOS transistor and PMOS transistor connected in parallel with a gate of the NMOS transistor being the first gate terminal of the first and second pass switches and a gate of the PMOS transistor being the second gate terminal of the first and second pass switches.

37. The method of claim 24 wherein in the mode switch comprises:

an interchip input/output pad connected to a first logic state generator during normal operation;

a test input/output pad connected to a second logic state generator during testing procedures.